430FX PCIset
82437FX (TSC) and 82438FX (TDP)
Specification Update

October 1997

Order Number: 297733-002

The Intel 430FX PCIset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update

CONTENTS

REVISION HISTORY

Date of Revision	Version	Description
July 1996	-001	Initial Release.
October 1997	-002	Moved PIIX issues to the PIIX/PIIX3 Spec Update. TSC/TDP remain in this document unchanged. Conversion to new template.

PREFACE

This document is an update to the specifications contained in the following documents:

Intel 82430FX PCIset Cache/Memory Subsystem Databook (Order number 290518)

Error! Reference source not found. Datasheet Addendum
(Order number 297463)

It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It contains Specification Changes, Errata, Specification Clarifications, Documentation Changes, and General Considerations and is divided into the following two parts:

- Part I: Specification Update for 82430FX (TSC)
- Part II: Specification Update 82430FX (TDP)

This document contains issues to only the current revision (stepping) of the TSC & TDP devices. In order to obtain issues known for earlier steppings of these components, contact your Intel Field Sales office.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the 430FX (TSC/TDP) behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

General Considerations include system level considerations that the system designer should account for when developing hardware or software products using the 82430FX (TSC) or 82430FX (TDP).

S-Specs are exceptions to the published specifications and apply only to the units assembled under that S-Spec.

Component Identification via Programming Interface (TSC)

PCI Register	PCI Offset	Value
Vendor ID	00-01h	8086h
Device ID	02-03h	122Dh
Revision Number	08h	01h (A-1 steppings) 02h (A-2 steppings)

Part I:

Specification Update for 430FX (TSC)

GENERAL INFORMATION

This section covers the 82437FX (TSC).

82437FX TSC

Stepping	S-Spec	Top Marking	Freq.	Notes
A-1	SZ966	SB82437FX-66, SZ966	66 MHz	Production
A-1	SZ973	SB82437FX-60, SZ973	60 MHz	Production
A-1	Q294	SB82437FX-66, Q294	66 MHz	ES
A-1	Q289	SB82437FX-60, Q289	60 MHz	ES
A-1	SZ968	SB82437FX-66, SZ968	66 MHz	Production
A-1	SZ975	SB82437FX-60, SZ975	60 MHz	Production
A-1	Q291	SB82437FX-66, Q291	66 MHz	ES
A-1	Q290	SB82437FX-60, Q290	60 MHz	ES
A-2	SZ999	SB82437FX-66, SZ999	66 MHz	Production
A-2	SZ998	SB82437FX-60, SZ998	60 MHz	Production
A-2	Q319	SB82437FX-66, Q319	66 MHz	ES
A-2	Q320	SB82437FX-60, Q320	60 MHz	ES

Summary Table of Changes

The following table indicates the Specification Changes, S-Specs, Errata, Specification Clarifications, Documentation Changes, or General Considerations which apply to the listed 430FX (TSC) steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This item is either new or modified from the previous version of the document.

82437FX TSC

NO.	A1	A2	Plans	SPECIFICATION CHANGES	Documentation Status
				There are currently no known 82437FX (TSC) Specification Changes	
NO.	**A1**	**A2**	**Plans**	**ERRATA**	**Documentation Status**
1	X			Lock Retry.	In this document
2	X	X	Doc	SMRAM Space Not Properly Decoded When 512K-640K Memory is Enabled.	In Rev 2 Datasheet, section 4.4.8
3	X	X	Doc	TSC Does Not Insert a Turnaround Cycle in Specific System Scenarios.	In Rev 2 Datasheet, section 4.6.1
NO.	**A1**	**A2**	**Plans**	**SPECIFICATION CLARIFICATIONS**	**Documentation Status**
1	X	X	Doc	Clarification on Flushing L2 Cache.	In Rev 2 Datasheet, section 4.3.4
2	X	X	Doc	NA# Connection and NA# Enable bit.	In Rev 2 Datasheet, section 3.2.11
3	X	X	Doc	BIOS Configuration of DRAM when using EDO DRAMs.	In Rev 2 Datasheet, section 4.4.5.1
4	X	X	Doc	REQ# Behavior.	In Rev 2 Datasheet, section 4.6.1.1
5	X	X	Doc	Read Modify Write Cycles to Write Protected Memory Not Supported.	In Rev 2 Datasheet, section 3.2.14

NO.	A1	A2	Plans	DOCUMENTATION CHANGES	Documentation Status
				There are currently no known 82437FX (TSC) Documentation Changes	
NO.	**A1**	**A2**	**Plans**	**GENERAL CONSIDERATIONS**	**Documentation Status**
1	X	X	Doc	Layout Considerations for TSC/TDP Control Signal Interface.	In this document
2	X	X	Doc	Invalid C/BE[3:0]# During Combined Incomplete Dword Bursting from CPU - PCI.	In this document

82437FX (TSC) SPECIFICATION CHANGES

There are currently no known 82437FX (TSC) Specification Changes.

82437FX (TSC) ERRATA

1. Locked PCI Cycles By TSC To Retrying PCI Target Do Not Function Properly

During 82430FX PCIset compatibility validation it was found that the TSC does not properly terminate LOCKed PCI cycles that are retried by a target PCI device. The failing system was configured with a certain PCI Graphics card, an audio card, and standard Microsoft® Windows™ VGA driver. In this configuration a system lock-up occurred. The failing scenario was (1) the TSC is retried on a locked access to this PCI Graphics card which was immediately followed by (2) an audio card DMA to main memory. The lock-up condition initiated when the TSC did not properly terminate the Locked PCI cycle which was retried by this PCI Graphics Card. Since the Locked cycle access was not properly terminated, the audio card DMA did not complete and thus the system lock-up occurred. System lock-up did not occur once the drivers supplied by the PCI Graphics Card vendor were installed since the vendor's VGA drivers do not cause the CPU to perform Locked cycles to PCI.

IMPLICATIONS: A specific Card that 1) incorporates the PCI Retry mechanism and *2)* that *is memory mapped* on the PCI bus and 3) has drivers or applications that create LOCKed accesses to this card can be susceptible to this erratum. An example of this type of card could be a PCI Graphics card. Typically cards that *are not* in this category are SCSI and LAN cards (which I/O map and therefore are not susceptible to this erratum) and other PCI Graphics cards which do not perform the retry function.

Dozens of PCI graphics cards which were tested as part of the 82430FX PCIset compatibility validation *did not* cause the system to lock-up when using the standard Windows VGA driver or when using the drivers supplied by the graphics card vendor. There were two cards, out of all these cards, that failed the test.

SILICON STATUS: This erratum was fixed in the A-2 stepping of the TSC.

WORKAROUND OPTIONS:

WORKAROUND #1: This is a software solution for a card that incorporates the Retry mechanism *and is memory mapped* on the PCI bus. When using a PCI Card which incorporates the Retry function, applications and/or drivers for this card must not create LOCKed accesses to this card. An example of this workaround would be to *replace* the Windows 3.1 standard VGA driver or the standard IBM® OS/2® driver which use the "XCHG" instruction. Typically *drivers supplied by the card vendor do not create* LOCKed cycles on PCI and therefore are not susceptible to this TSC erratum from the driver.

WORKAROUND #2: This is a hardware solution which incorporates a 24 Pin PLD, type 22V10-7 (7.5 ns combinatorial throughput), onto the motherboard. The PLD implements a blocking mechanism which allows the TSC to successfully complete the LOCKed PCI transaction cycle to the retrying PCI target. Complete soft copy documentation is available from your Intel Field Sales office. The documentation file is called "TRI_PLD1.EXE", a self extracting file that contains a state diagram and a separate .ABL file. The .ABL file includes the PLD equations. Implementing this workaround will ensure that the locked retry function in the PCI specification can be performed.

* All other trademarks are property of their respective owners.

STATUS: For the steppings affected see the *Summary Table of Changes* at the beginning of this section.

2. SMRAM Space Not Properly Decoded By TSC When 512K-640K Memory Hole is Enabled

During 82430FX compatibility validation it was found that the TSC does not properly decode SMM DRAM Space when the TSC 512K-640K Memory Hole is enabled. If the 512K-640K Memory Hole is enabled, the TSC incorrectly extends the hole into the SMRAM space. Cards requiring the use of the 512K-640K memory hole are very limited. The TSC will properly decode memory space in any other circumstance.

IMPLICATIONS: A system using system management mode interrupts with addresses directed to SMM memory space in segments A0000h and B0000h will not function properly if the 512K-640K memory hole is enabled. Systems in this configuration will have the TSC SMRAM register at 72h configured and will have the TSC DRAMC register 57h bits [7:6] set to 01b.

SILICON STATUS: This erratum will not be fixed in the next stepping of the TSC.

WORKAROUND : Cards requiring the use of the 512K-640K memory hole are very limited. For those cards using the 512K-640K memory hole and SMM as described above, the optional 15M-16M memory hole is available. The TSC 15M-16M memory hole is enabled at TSC DRAMC register 57h bits [7:6] set to 10b.

STATUS: For the steppings affected see the *Summary Table of Changes* at the beginning of this section.

3. TSC Does Not Insert a Turnaround Cycle Under Specific System Scenarios

During Post-Silicon system level simulation a specific system scenario was found that involves a TSC turnaround cycle. The simulation revealed that if a PCI master had been requesting the PCI bus for some time and the TSC has just flushed its CPU-to-PCI write posting buffers, the TSC could grant to a master the bus one clock early. Under any other circumstance the TSC grants the bus to the requesting master such that the TSC floats the bus one clock before a master can start driving the bus. *No system failures or effects have been reported as a result of this issue.*

IMPLICATIONS: For the scenario described above, the TSC can be in the process of floating it's output buffers while a newly granted PCI master is starting to drive the bus. Therefore, some contention may be possible on the AD[31:0], C/BE[3:0]# and PAR lines. Any possible contention, however, is very limited due to the TSC's max float delay timing of 8.5 ns.

SILICON STATUS: No fix is planned for this erratum.

WORKAROUND: *A workaround is not recommended.* For more detailed information, Intel has prepared a white paper titled "Analysis of TSC Turnaround Issue." This document is available from your Local Intel Sales Office.

STATUS: For the steppings affected see the *Summary Table of Changes* at the beginning of this section.

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82437FX (TSC) SPECIFICATION CLARIFICATIONS

1. Clarification on how to Flush the L2 cache.

The SCFMI (Force Miss/Invalidate) mode is intended to allow flushing of dirty L2 lines back to memory. The mode works as defined. Since the flushed dirty line is posted to the DRAM write buffer in parallel with the linefill, the new line (which is filled to both L1 and L2) is guaranteed to be stale data.

The implication of the actual operation is that any program that is attempting to flush the L2 must not be run from the L2 itself, unless the L2 code image is coherent with DRAM. For example, if a DOS program to flush the L2 is loaded, it is loaded from disk using a string move. The MOVS may result in loading the program partially into L2, since the memory writes will (likely) hit previously valid lines in the L2. When the flush program sets the SCFMI bit to force misses, subsequent code fetches may be serviced from L2 which contain the stale code image.

An important aspect to consider when flushing L2 is to ensure that the code being used to flush the cache is not in the current 256K page (256K L2 being used here) residing in L2. The BIOS algorithm will also work if it is executed from non-cacheable or write-protected DRAM space (e.g. BIOS region). If this can't be guaranteed, then an alternate software flush algorithm is to read 2X the size of the L2. Note that this implies a protected-mode code for the 512K L2 case.

2. Pipelining: NA# Connection and NA# Enable Bit in TSC

The NA# signal can be connected or disconnected from the processor as long as the"NA Disable" bit is set to a "1" if the NA# signal is disconnected from the processor. The NA Disable bit is located in the TSC Cache Control Register, address offset 052h, bit 3. When bit 3 is"1" the TSCs NA# signal is never asserted. When bit 3 is "0" NA# will be asserted as appropriate by the TSC. The NA# disable bit defaults to where the TSC can assert NA#, i.e. reset to "0". The NA# disable bit should be set appropriately before either L1 or L2 is enabled.

3. BIOS Configuration of DRAM Array when using EDO DRAMs

The following algorithm should be followed in order to dynamically detect if EDO DRAMs are installed in the system. When this algorithm has completed, the DRAM type installed in each row is programmed into the DRAM Row Type register (TSC PCI Config. Offset 68h):

1. Initialize all of the DRAM Row Type values to 'EDO' in the DRT register (TSC PCI Config. Offset 68h.) Since there are five rows, the DRT register value becomes '1Fh'.

2. For each bank row (Row1, Row2, Row3, Row4, Row5)

- Write all '1's to a QWORD address within the row.
- Enable EDO detection mode by setting the EDO Detect Mode Enable bit in the DRAMC register (TSC PCI Config. Offset 57h) to '1'.
- Immediately read back the value of the QWORD address.
- If the value is not all '1's, then standard page mode DRAMs are installed in that row. Otherwise the EDO mode DRAMs are installed in that row.
- Disable EDO detection mode by clearing the EDO Detect Mode Enable bit in the DRAMC register

3. Depending on the findings of Step #2, program the DRAM row type into the corresponding bit in the DRT register (TSC PCI Config. Offset 68h): set for EDO type ('1') or reset for standard page mode ('0'.) Do not program this register until all of the bank rows have been tested.

Once all DRAM row banks have been tested for EDO, the EDME bit should be cleared in DRAMC. (TSC PCI Config. Offset 57h, bit 2 is '0') It is very important that the EDME bit be cleared afterwards or performance will be seriously impacted.

4. Arbitration Signaling Protocol: REQ# Functionality

PCI Masters should follow the intent of the PCI Specification as quoted from the PCI Specification below:

1. "Agents must only use REQ# to signal a true need to use the bus."
2. "An Agent must never use REQ# to "park" itself on the bus."

A "well behaved" card should use REQ# when the bus is really needed. Typically REQ# should be removed, once the PCI master has been granted the bus, after FRAME# is asserted. Currently, PCI Cards tested in Intel's compatibility labs appear to have the proper REQ# functionality.

REQ# line behavior, of future PCI Cards, that *may not* operate as required could include:

1. Glitching REQ# lines for 1 or more clocks without any apparent reason
2. Glitching REQ# lines and then not waiting for GNT# assertion
3. Continually asserting REQ# lines in an attempt to park itself on the PCI bus.
4. Failing to assert FRAME# within several clocks of GNT# assertion when bus is idle.

PCI Cards that do not operate properly may not function properly with the TSC.

5. Read-Modify-Write Cycles to Write Protected Memory Not Supported

The 82430FX PCIset does not support read-modify-write cycles to memory space defined by the Programmable Attribute Map registers as *write protected*. System software should not perform read-modify-write cycles to areas that it has previously write protected.

82437FX (TSC) DOCUMENTATION CHANGES

There are currently no known 82437FX (TSC) Documentation Changes.

82437FX (TSC) GENERAL CONSIDERATIONS

1. Layout Considerations for TSC/TDP Control Signal Interface

When laying out a 82430FX PCIset design for robust 66 MHz operation, considerations must be made for the following control signals: MOE#, MADV#, HOE#, and POE#. These control signals should be routed from the TSC to the TDPs such that the TDPs are symmetrically "T"d off. This suggested route is similar to the recommended HCLK routing for the TDPs. Additionally, the MOE# signals '245 buffer should be placed in-between the TDPs and TSC.

If traces from the TSC to the TDP are longer than 5 inches, 22 ohm series damping resistors will be required to ensure signal integrity. These series damping resistors should be placed in close proximity to the TSC. Failure to implement these recommendations could result in signal integrity issues such as noise spikes.

2. Invalid C/BE# during combined Incomplete Dword bursting from CPU to PCI. *Applies to all TSC steppings.*

When the TSC is combining incomplete Dwords from the CPU for bursting onto PCI, the TSC may not properly control the value of C/BE#'s as per PCI Specification 2.0. During multiple CPU writes of incomplete Dwords to PCI, the TSC can combine these into a burst transaction. In some cases, during these bursts, the TSC will insert wait state(s) and provide the C/BE# value on the data phase*after* this wait state. The PCI Specification 2.0 requires that these C/BE#'s have the correct data on the clock following the consummation of the previous data phase. Add-in cards sampling C/BE#'s during a wait state in this circumstance will not work. Two workarounds are available. 1) Disable CPU to PCI Write Bursting (Reg 50h) --***Not Suggested.*** or, 2) Sample C/BE#'s when IRDY# & TRDY# asserted -- ***Suggested***

Part II:

Specification Update for 82378FX (TDP)

GENERAL INFORMATION

82438FX TDP

Stepping	S-Spec	Top Marking	Freq.	Notes
A-0	Q259	SB82438FX, Q259	66 MHz	ES
A-0	Q270	SB82438FX, Q270	66 MHz	ES
A-1	SZ965	SB82438FX, SZ965	66 MHz	Production
A-1	Q292	SB82438FX, Q292	66 MHz	ES
A-1	SZ969	SB82438FX, SZ969	66 MHz	Production
A-1	Q259	SB82438FX, Q259	66 MHz	ES

Summary Table of Changes

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Shaded:	This item is either new or modified from the previous version of the document.

82378FX (TDP)

NO.	A1	A2	Plans	SPECIFICATION CHANGES	Documentation Status
				There are currently no known 82438FX (TDP) Specification Changes	
NO.	**A1**	**A2**	**Plans**	**ERRATA**	**Documentation Status**
				There are currently no known 82438FX (TDP) Errata	
NO.	**A1**	**A2**	**Plans**	**SPECIFICATION CLARIFICATIONS**	**Documentation Status**
				There are currently no known 82438FX (TDP) Specification Clarifications	
NO.	**A1**	**A2**	**Plans**	**DOCUMENTATION CHANGES**	**Documentation Status**
				There are currently no known 82438FX (TDP) Documentation Changes	
NO.	**A1**	**A2**	**Plans**	**GENERAL CONSIDERATIONS**	**Documentation Status**
				There are currently no known 82438FX (TDP) General Considerations	

82378FX (TDP) SPECIFICATION CHANGES

There are currently no known 82378FX (TDP) Specification Changes.82378FX (TDP) ERRATA

82378FX (TDP) ERRATA

There are currently no known 82378 (TDP) Errata.

82378FX (TDP) SPECIFICATION CLARIFICATIONS

There are currently no known 82378FX (TDP) Specification Clarifications.82378FX (TDP)

82378FX (TDP) DOCUMENTATION CHANGES

There are currently no known 82378FX (TDP) Documentation Changes.82378FX (TDP)

82378FX (TDP) GENERAL CONSIDERATIONS

Refer to TSC General Considerations, Layout Considerations for TSC/TDP Control Signals

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